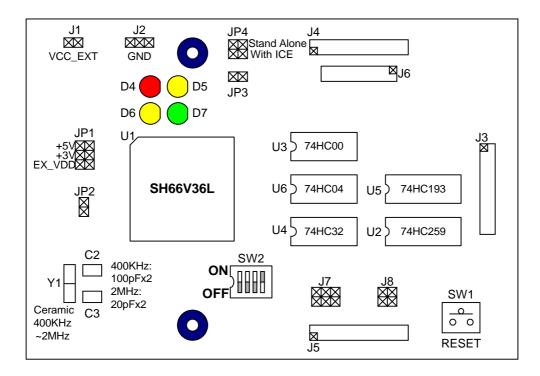


SH6636 EVB

Application Notice for SH6636 EVB

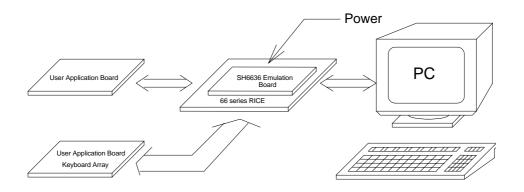
SH6636 EVB

The SH6636 EVB is used to evaluate the SH6636 chip's function for the development of application program. It contains of a SH66V36 chip to evaluate the functions of SH6636 including the infrared remote control transmitter function. The following figure shows the placement diagram of SH6636 EVB.



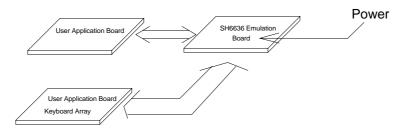


There are two configurations of SH6636 EVB in application development: ICE mode and stand-alone mode. In the ICE mode, the SH66xx ICE (motherboard) is connected to the SH6636 EVB by the ICE interface.



(a) ICE mode

In the standalone mode, the SH6636 EVB is no longer connected to the motherboard. But the EPROM board has must be connected to the SH6636 EVB by the EPROM interface. The EPROM store the application program; they may be the 27512.



(b) Stand-alone mode

The process of your program's evaluation on SH6636 EVB

Uasm66.exe: assemble the program, and get binary (*.obj) file and the other files. Depart the one 16 bits obj file to the two 8 bit files by convert.exe.

Usage example (for example: aaa.asm):

- 1.Run the SH66 series assemble program:
 - C: >uasm66 aaa.asm ; to produce the obj file: aaa.obj
- 2. Depart the aaa.obj to two 8-bit file aaah.obj and aaal.obj, for example:
- C: > convert
 - Input the 16 bits (.obj) file aaa.obj
 - Then aaah.obj and aaal.obj will be created.
- 3. Write the aaah.obj to EPROM (ROMH)
- Write the aaal.obj to EPROM (ROML)
- 4. Put the two EPROM (ROML and ROMH) on the EPROM board.
- 5. Then put the EPROM board on the EVB by J6, J7 and J8.



SH6636 EVB

ROM bank switch application Notice

The ROM of SH6636 is divided to 2K banks. There are 12 banks in this 24K ROM.

CPU Address	ROM Space										
	BNK=0	BNK=1	BNK=2	BNK=3	BNK=4	BNK=5	BNK=6	BNK=7	BNK=8	BNK=9	BNK=A
000 ~ 7FF	0000 ~ 07FF	0000 ~ 07FF (BANK 0)									
800 ~ FFF	0800 ~ 0FFF	1000 ~ 17FF	1800 ~ 1FFF	2000 ~ 27FF	2800 ~ 2FFF	3000 ~ 37FF	3800 ~ 3FFF	4000 ~ 47FF	4800 ~ 4FFF	(BANK 0) 5000 ~ 57FF (BANK 10)	(BANK 0) 5800 ~ 5FFF (BANK 11)

Bank switch program example:

<u>Example 1:</u> BANK0:ORG 000H; bank 0 program

BANK EQU 1FH BANK2 EQU 1H

LDI BANK, BANK2 JMP 1000H; from bank0 jump to bank2

BANK2:ORG 1000H; bank2

•••

Example 2:

Program1: BANK1:... BANK EQU 1FH BANK4 EQU 3H

LDI BANK, BANK4 JMP B4SR1

Program 2: BANK4: ORG 2000H B4SR1:

••••



SH6636 EVB Programming Notices:

- 1. Clear data RAM and initialize all system registers at the beginning.
- 2. Do not perform logical operation with I/O ports. Especially when the I/O ports have external connections.
- 3. Do not perform arithmetic operation with those registers only have 1, 2 or 3 bit. This kind of operation may not get the result you expected.
- 4. Never use reserved registers.
- 5. Keep enable (default) or disable of the LPD circuit. If it has been disabled, nevermore enable with the software control.
- 6. If "IE" instruction (interrupt enable) is set outside the interrupt processing program and there is "HALT" or "STOP" instruction, this two instructions should be followed "IE" instruction closely.
- 7. After CPU responding to an interrupt, IRQ should be cleared before resetting IE in order to avoid many responses to one interrupt.
- 8. Interrupt Enable instruction will be automatically cleared after entering interrupt-processing program. If setting IE too early, there is a possibility of re-entry the interrupt. So the Interrupt Enable instruction should be placed at the end and followed closely by two instructions include "RTNI".
- 9. During the two successive instruction cycles next to Interrupt Enable instruction, CPU will not respond to any interrupts.
- 10. After CPU responding to interrupts, each bit of IE will be cleared by hardware while IRQ should be cleared by software.
- 11. It is necessary to add NOP before or after the HALT instruction, else the CPU will execute error instruction when it wakes up from the HALT.

. . NOP HALT NOP

- 12. It is wise to set Interrupt Enable flag before you return from subroutine in two instructions.
 - LDI IE, 04H ; Enable timer0 interrupt LDA Temp, 0 RTNI
- 13. When you set interrupt enable flag as the following and your subroutine do not set Interrupt Enable flag, then your system will never wake up if an interrupt entered between the NOP.

LDI IE, 1111B; IE = Interrupt enable flag NOP NOP NOP HALT

- 14. To add "p=6636" and "romsize=24576" at the beginning of a program. If found problem in compiling the program. Check if the SH6566.dev is located at the program directory.
- 15. Interrupt must be disabled when bank is switching. Otherwise, the program may be failed.

```
LDI IE, 0000B; IE = Interrupt enable/disable flag
NOP
NOP
LDI IFH,03H
JMP LABEL1
```

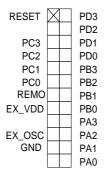
- 16. Shared interrupt program can be stored in BANK0. When the program runs in other BANK while an interrupt comes, it will automatically jump to the interrupt program in BANK0 and can return to the current BANK automatically after returning from the interrupt.
- 17. When setting Timer Counter, first fill TOL, then TOH.
- 18. After setting TM0, TOL, TOH, it is unnecessary to reset them after interrupt each time. If TM0, TOL, TOH are reset after each TIMER interrupt, interrupt interval time will not equal because the interrupt timing is not successive.



- 19. Any instruction containing writing to or reading form memory, it should not be used to operate with I/O Port. It is best to avoid using those instructions such as "SUB, ADD " which do not contain Write operation with I/O Port but have computation operation.
- 20. "1" must be written to I/O Port before Reading.
- 21. Writing "1" to I/O Open Drain and then entering "STOP" will cause current leakage ranging from tens to hundreds micro-ampere. So pull up or pull down resistors value from 1 to 2 MΩ must be used to prevent I/O Float when I/O in Open Drain mode.
- 22. Directly reading PORT states ensure the count is correct.
- 23. Interrupt activating from STOP at the first time can save power.
- 24. When the Compiler of old version compiles program, the last line will be read twice. So, if the last line is an instruction, two same operations will be occurred. If there is Label in the last line, compiler will give an error named 'repeated definition'. This will happen in main program or included files and it is recommended that the last line should be a blank line or END.
- 25. The stack has four layers, if an interrupt is enabled, there only have three layers can be used. Otherwise, if an interrupt comes, the stack will be overflowed that will cause CPU Reset or other errors.
- 26. Key De-bounce time is recommended to be 50ms. If a user use Rubber Key, it is best to test Rubber Key's Debounce time.
- 27. Index register DPH and DPM both have three bits only, so pay attention to the referred address when using them.
- 28. The "NOP" instruction should be added at the beginning of the program to ensure the IC is stability.



SH6636 interface connector: J3 (Top View from EVB)



External Vcc input:

J1, J2:

The external power input when the EV Board worked in stand-alone mode. The voltage of VCC_EXT must be 5V±5%.

Jumper setting:

JP1 (SH66V36 chip power select):

- If short the +5V positions, the voltage (+5V) of SH66V36 is internal source.
- If short the +3V positions, the voltage (+3V) of SH66V36 is internal source.
- If short the EX_VDD positions, you can external input the power (2.0~5.0V, refer to SH6636 spec) of SH66V36 from EX_VDD.

JP2 (SH66V36 chip power import):

- This jumper must be connecting.
- If you want to get the operating current (for reference only), remove the jump and link a current-meter.

JP3:

■ This jumper must be connecting.

JP4 (SH6636 EVB ICE/Stand-alone mode select):

- If you short there "with ICE" positions, the clock of SH6636 EVB is fed from ICE. This is only for ICE mode.
- If you short the "Stand alone" positions, the clock (Ceramic 400KHz~2MHz) of SH66V36 is put on Y1 on board by yourself. This is only for stand-alone mode.

Switch setting:

SW1:

■ Reset the whole system when push the button.

SW2:

- Bit1& Bit3 are turn off.
- Bit2: Warm-up counter ON/OFF switch.

The warm-up counter will on when it is turn off.(Default)

- Bit4: STACK overflow ON/OFF switch.
 - The stack overflow function in ICE mode will on when it is turn on.(Default)

LED declare:

STOP indicate:

D4 is lighted when the system has gone into the STOP mode.

HALT indicate:

D5 is lighted when the system has gone into the HALT mode.

Port pull up indicate:

D6 is lighted when port pull up enable.

LPD indicate:

D7 is lighted when LPD enable.



Notice:

Evaluate your program with ICE indicate:

- 1. After enter to RICE66 and successfully download the user program, push the F5 (Reset) on PC keyboard before run your program when you evaluate your program with ICE. If there were abnormal response, the user should power off the ICE, quit RICE66 and wait for a few seconds before restart.
- 2. First time run RICE66, need to select an appropriate MCU type, clock frequency ... save the settings and restart RICE66 again.
- 3. Can't Step (F8) or Over (F9) a HALT and STOP instruction.
- 4. When you want to escape from HALT or STOP (in ICE mode), you should press the F5 key on PC keyboard twice.
- 5. The maximum current limit of the 3V power is 100mA, when the user uses internal 3V power to drive external device such as LED.
- 6. When EV. Board worked in "with ICE" mode, you can input the clock from EX_OSC as the system clock. (refer to the RICE66 User's Guide)