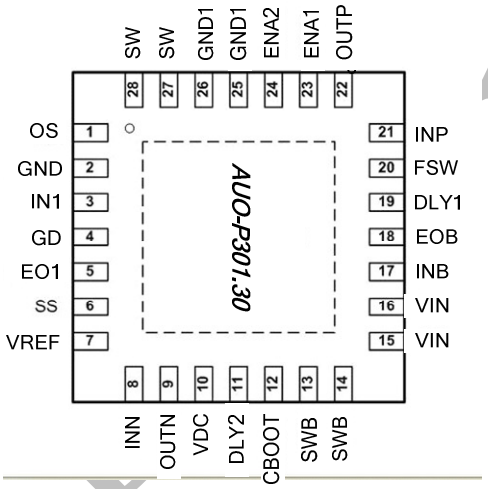
4-CHANNEL TFT LCD POWER SOLUTION WITH ADJUSTABLE DELAY CONTROL

FEATURES

- **9.5V to 14V Input Voltage Range**
- **Built in 3.5A, 0.15Ω Switching NMOS for AVDD**
- **Built in 2.5A, 0.25Ω Switching NMOS for VLogic**
- **VGH Linear Regulator Up to 40V/50mA**
- **VGL Linear Regulator Down to –14V/50mA**
- **Adjustable Power On Sequencing**
- **750kHz Fixed Switching Frequency for VLogic**
- **Adjustable Switching Frequency 500k~2000kHz for Boost**
- **GD Function for Driving External PMOS**
- **WQFN28- 5mm*5mm Package Available**

PIN CONFIGURATION



GENERAL DESCRIPTION

The AUO-P301.30 is a 4-channel TFT LCD power solution which provides a step-up PWM controller (AVDD), a step-down PWM (VLogic), and two high voltage Linear Regulators for VGH and VGL. By controlling ENA and connecting two external capacitors to DLY1, DLY2, the best power up sequencing of AUO-P301.30 can be achieved GD is the open drain output signal which goes low when the VIN is larger than UVLO. Connecting GD to an extra PMOS transistor can keep AVDD low before AVDD_F is ready. AUO-P301.30 also have protect mechanisms such as over voltage protect (OVP), over current protect (OCP), output under voltage protect (UVP) and thermal protect.

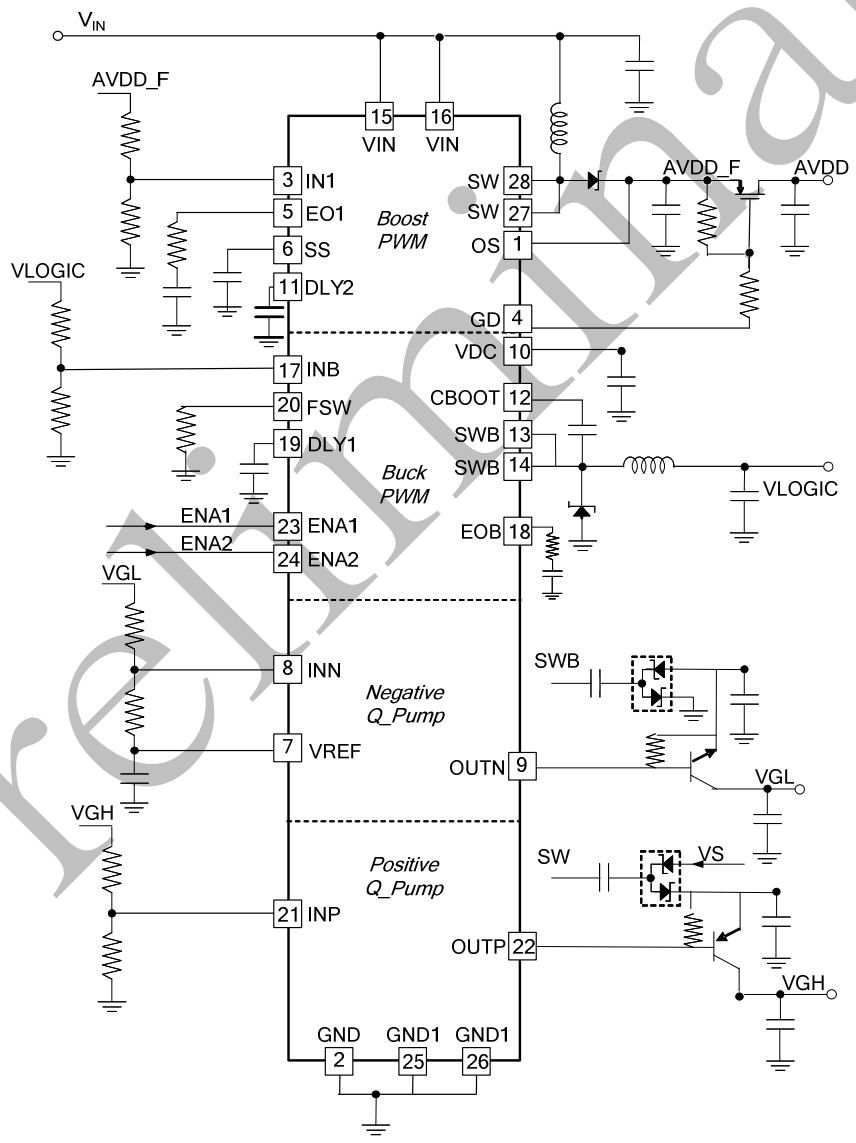
With the minimal external components, the AUO-P301.30 offers a simple and economical solution for TFT LCD TV power solution.

ORDERING INFORMATION

DEVICE TYPE	PART NUMBER	PACKAGE	PACKING	TEMP. RANGE	MARKING	MARKING DESCRIPTION
AUO-P301.30	AUO-P30 1.30-Q20-T	Q20: WQFN28-5 X5	T: Tape and Reel	–40°C to +85°C	AUO-P301.30 XXXXXX XXXX	1. Part Name 2. Lot No. (6~9 Digits) 3. Date Code (4 Digits)

Note: All AAT products are lead free and halogen free.

TYPICAL APPLICATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
VIN, to GND	V_{DD}	16.5	V
VDC to GND	V_{LV}	7	V
SW, OS, GD to GND	V_{H1}	22	V
CBOOT to GND	V_{H2}	20	V
SWB to GND	V_{H3}	V_{H2} +0.3	V
OUTP to GND	V_{H4}	40	V
OUTN to GND	V_{H5}	–20	V
Input Voltage 1 (ENA1, ENA2)	V_{I1}	V_{DD} +0.3	V
Input Voltage 2 (DLY1, IN1, INB, INN, INP, SS, DLY1, DLY2)	V_{I3}	V_{LV} +0.3	V
Output Voltage 2 (EOB, EO1, VSET, VREF, fsw)	V_{O2}	–0.3 to (V_{LV} +0.3)	V
Operating Ambient Temperature Range	T_C	–40 to +85	°C
Operating Junction Temperature Range	T_J	–40 to +150	°C
Storage Temperature Range	$T_{STORAGE}$	–65 to +150	°C
Package Thermal Resistance	θ_{JA}	34	°C /W
Power Dissipation, @ T_C = +25°C , T_J = +125°C	P_d	2.941	W

Note: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended period of time may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 9.5V to 14V, T_C = –40°C to +85°C , unless otherwise specified. Typical values are tested at +25°C ambient temperature, V_{IN} = 12V, V_{DD1} = 15.7V.)

Operating Condition

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
VIN Input Voltage Range	V_{DD}		9.5	-	14.0	V
OS Input Voltage Range	V_{DD1}		9.5	-	19.0	V
VIN Operating Current	I_{VDD}	$V_{IN1/INB}$ = 1.5V, Not Switching	-	2	5	mA
		$V_{IN1/INB}$ = 1.0V, Switching	-	6	10	mA
VIN Under Voltage Lockout	V_{UVLO}	VIN Rising	-	7.9	8.66	V
		VIN Falling	6.84	7.60	-	V
Thermal Shutdown	T_{SHDN}		-	160	-	°C

Reference Voltage and Oscillator

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Reference Voltage	V_{REF}	$I_{V_{REF}}$ = 100µA	1.23	1.25	1.27	V
Line Regulation		$I_{V_{REF}}$ = 100µA	-	2	5	%/V
Load regulation		$I_{V_{REF}}$ = 0~100µA	-	1	5	%/mA

ELECTRICAL CHARACTERISTICS

(V_{IN} = 9.5V to 14V, T_C = –40 °C to +85 °C , unless otherwise specified. Typical values are tested at +25 °C ambient temperature, V_{IN} = 12V, V_{DD1} = 15.7V.)

Soft Start, Delay, Fault protect and Gate control Signal

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Soft Start Source Current	I_{SS}	$V_{THRESHOLD}$ = 1.25V	6	9	12	µA
DLY1 Source Current	I_{DLY1}	$V_{THRESHOLD}$ = 1.25V	3.6	5.0	6.4	µA
DLY2 Source Current	I_{DLY2}	$V_{THRESHOLD}$ = 1.25V	3.6	5.0	6.4	µA
BUCK Soft Start Period	T_{SSB1}		-	1.5	3.0	mS
Gate On Voltage (VGH) Soft Start Period	T_{SSP}		-	8	16	mS
Gate OFF Voltage (VGL) Soft Start Period	T_{SSN}		-	8	16	mS
During Fault Protect Trigger Time	T_{FP}		180	200	220-	mS
IN1 Fault Trigger Level	V_{F1}		1.02	1.08	1.12	V
INB Fault Trigger Level	V_{FB1}		1.02	1.08	1.12	V
INP Fault Trigger Level	V_{FP}		1.02	1.08	1.12	V
INN Fault Trigger Level	V_{FN}		-	0.4	-	V
GD Leakage Current	I_{GD_leak}	V_{GD} = 19.5V	-	-	1	µA
GD Pull Down Threshold Voltage	V_{GD_tri}		0.88* VDD1	0.92* VDD1	0.96* VDD1	V
GD Pull Down Low Voltage	V_{GD_Low}	IGD=500µA	-	-	0.3	V

Logic Signal (ENA1, ENA2)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
High Level Input Voltage	V_{IH}		1.75	-	-	V
Low Level Input Voltage	I_{IL}		-	-	0.75	V
Input Bias Current	I_{IB}	$V_{ENA,\ FREQ}$ = 0 to VIN	–40	0	+40	nA

ELECTRICAL CHARACTERISTICS

(V_{IN} = 9.5V to 14V, T_C = –40°C to +85°C , unless otherwise specified. Typical values are tested at +25°C ambient temperature, V_{IN} = 12V, V_{DD1} = 15.7V.)

Oscillator

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Oscillation Frequency	f_{OSC_Buck}	Fixed for Buck	600	750	900	kHz
	f_{OSC_Boost}	Boost F_{SW} = 50k	1,600	2,000	2,400	kHz
		Boost F_{SW} = 66.66k	1200	1,500	1,800	kHz
		Boost F_{SW} = 83k	960	1,200	1,440	kHz
		Boost F_{SW} = 133k	600	750	900	kHz
		Boost F_{SW} = 200k	400	500	600	kHz
Maximum Duty Cycle	D_{MAX}	Boost PWM	85	90	95	%
		Buck PWM	85	90	95	%

Buck PWM (VLOGIC)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Output Voltage Range	V_{LOGIC}		1.8	-	5.0	V
Feedback Voltage	V_{INB1}		1.23	1.25	1.27	V
Input Bias Current	I_{IBB1}	V_{INB1} = 1V to 1.5V	–40	0	+40	nA
Feedback-Voltage Line Regulation			-	0.05	0.15	%/V
NMOS Current Limit	I_{LIMB1}		2.5	-	-	A
NMOS On-Resistance	R_{ONB1}	I_{SWB} = 1.0A	-	0.25	-	Ω
NMOS Leakage Current	I_{SW1OFF}	V_{SWB} = 0V	-	0.01	5.00	μA

ELECTRICAL CHARACTERISTICS

(V_{IN} = 9.5V to 14V, T_C = –40°C to +85°C , unless otherwise specified. Typical values are tested at +25°C ambient temperature, V_{IN} = 12V, V_{DD1} = 15.7V.)

Boost PWM (AVDD)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Output Voltage Range	AVDD		-	-	19	V
AVDD Over Voltage Protect	V_{OVP}	Rising	-	20.5	21.5	V
		Falling	18.5	19.5	-	V
Feedback Voltage	V_{IN1}		1.23	1.25	1.27	V
Input Bias Current	I_{IB1}	V_{IN1} = 1V to 1.5V	–40	0	+40	nA
Feedback-Voltage Line Regulation		9.5V < V_{IN} < 12V	-	0.05	0.15	%/V
NMOS Current Limit	I_{LIM1}		3.5-	-	-	A
NMOS On-Resistance	R_{ON1}	I_{SW} = 1.0A	-	0.15	-	Ω
NMOS Leakage Current	I_{SWOFF}	V_{SW} = 19V	-	0.01	5.00	μA

Negative Charge Pump Linear Regulator (VGL)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
INN Feedback Voltage	V_{INN}		0.17	0.20	0.23	V
INN Input Bias Current	I_{IBN}	V_{INN} = –0.25V to 0.25V	–40	0	+40	nA
OUTN Leakage Current	I_{OFFN}	V_{INN} = 0V, V_{OUTN} = –6V	-	-	–5	μA
OUTN Source Current	I_{OUTN}	V_{INN} = 0.35V, V_{OUT2} = –6V	8	10	-	mA

ELECTRICAL CHARACTERISTICS

(V_{IN} = 9.5V to 14V, T_C = –40°C to +85°C , unless otherwise specified. Typical values are tested at +25°C ambient temperature, V_{IN} = 12V, V_{DD1} = 15.7V.)

Positive Charge Pump Linear Regulator (VGH)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
INP Feedback Voltage	V_{INP}		1.23	1.25	1.27	V
INP Input Bias Current	I_{IBP}	V_{INP} = 1V to 1.5V	–40	0	+40	nA
OUTP Leakage Current	I_{OFF3}	V_{INP} = 1.4V, V_{OUTP} = 34V	-	-	5	µA
OUTP Sink Current	I_{OUT3}	V_{INP} = 1.1V, V_{OUTP} = 25V	8	10	-	mA

PIN DESCRIPTION

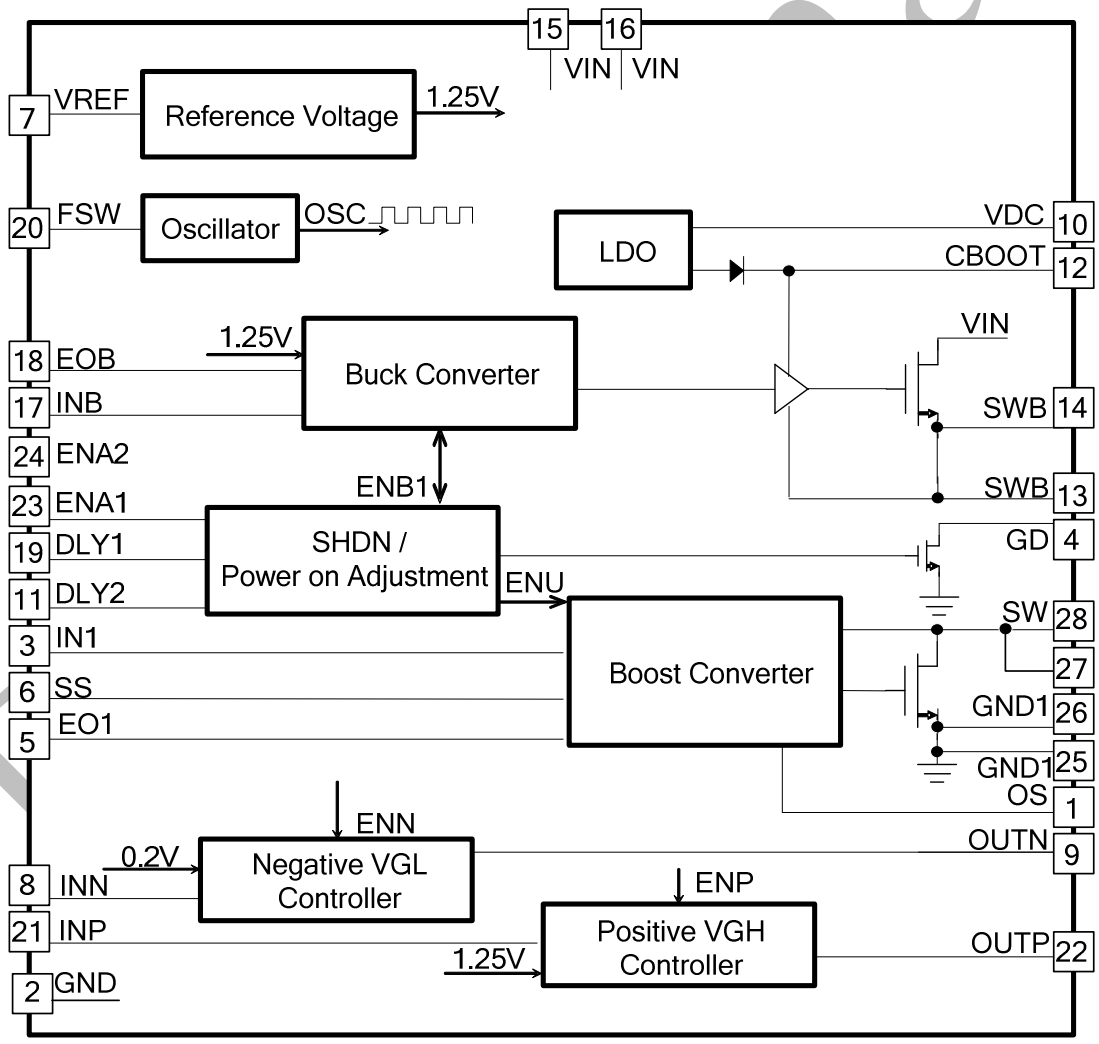
PIN NO. WQFN28	NAME	I/O	DESCRIPTION
1	OS	-	Step-up PWM Output Sensing Pin
2	GND	-	IC Ground
3	IN1	I	Step-up PWM Feedback Input
4	GD	O	Gate Driver for External Fault Protect PMOS
5	EO1	O	Step-up PWM Error Amplifier Output Pin
6	SS	I	Step-Up PWM Soft Start Control
7	VREF	O	Reference Voltage Output
8	INN	I	VGL LDO Controller Feedback Input
9	OUTN	O	VGL LDO Controller Output
10	VDC	O	Internal LDO Output Pin
11	DLY2	I	Power up Delay between ENA1 and VGH
12	CBOOT	O	Gate Driver Voltage for Step-down PWM Power MOS
13	SWB	O	Step-down PWM Power MOS Switching Pin
14	SWB	O	Step-down PWM Power MOS Switching Pin
15	VIN	-	Power Input
16	VIN	-	Power Input
17	INB	I	Step-down PWM Feedback Input
18	EOB	O	Step-down PWM Error Amplifier Output Pin
19	DLY1	I	Power up Delay between ENA1 and GD
20	FSW	O	Step-up PWM Switching Frequency Select Pin
21	INP	I	VGH LDO Controller Feedback Input
22	OUTP	O	VGH LDO Controller Output
23	ENA1	I	Step-up PWM Enable Pin (When ENA2 is High)

PIN DESCRIPTION

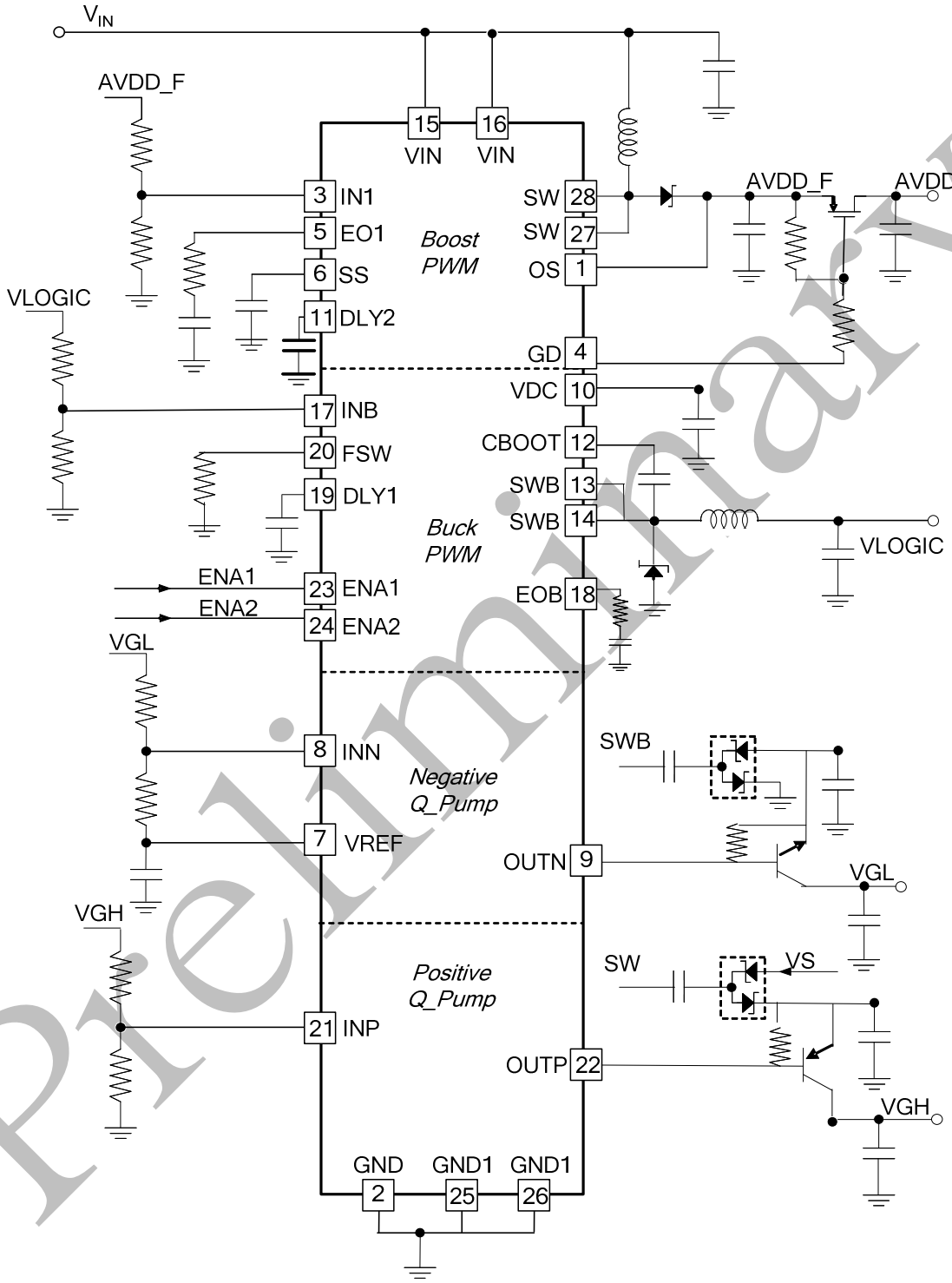
PIN NO. WQFN28	NAME	I/O	DESCRIPTION
24	ENA2	I	Step-down PWM Enable Pin
25	GND1	-	Step-up PWM Power MOS Ground
26	GND1	-	Step-up PWM Power MOS Ground
27	SW	O	Step-up PWM Power MOS Switching Pin
28	SW	O	Step-up PWM Power MOS Switching Pin

FUNCTION BLOCK DIAGRAM

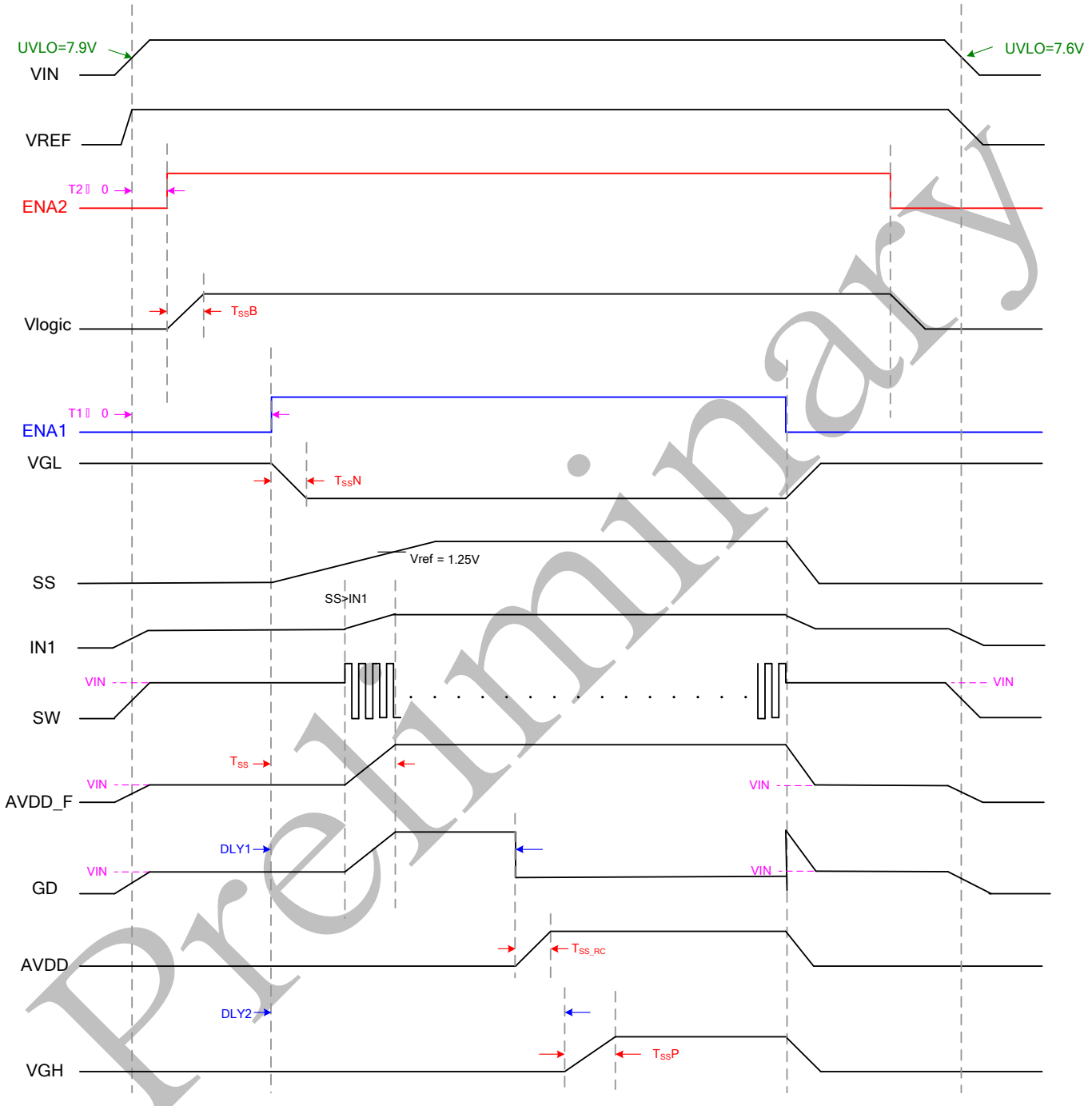
AUO-P301.30



TYPICAL APPLICATION CIRCUIT



TIMING WAVEFORM



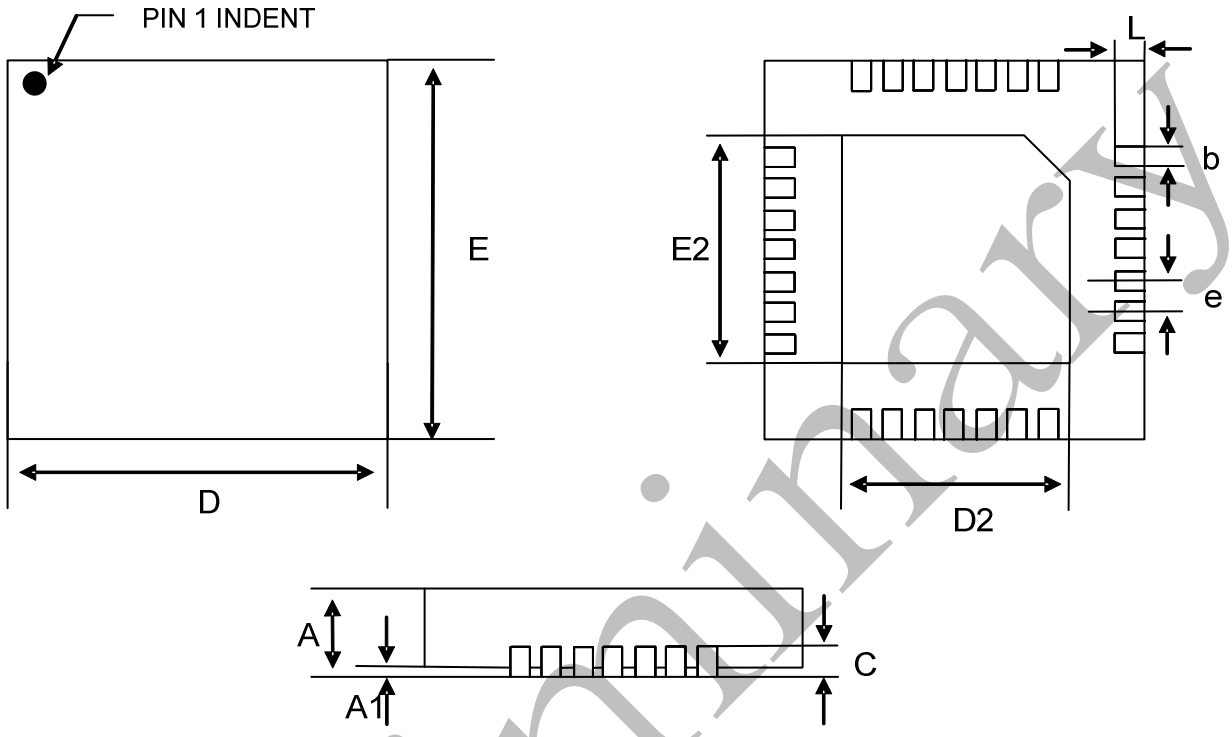
Note 1. T1≧T2

Note 2. ENA1 enable VGL and boost converter, ENA2 enable buck converter

Note 3. DLY1 set delay time between ENA1 and GD, DLY2 set delay time between ENA1 and VGH

PACKAGE DIMENSION

WQFN28-5X5



Symbol	Dimensions In Millimeters		
	MIN	TYP	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
C	0.19	0.20	0.25
D	4.95	5.00	5.05
D2	3.60	3.65	3.70
E	4.95	5.00	5.05
E2	3.60	3.65	3.70
e	-----	0.50	-----
L	0.35	0.40	0.45